NISHAD SARAF

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PROFESSIONAL SUMMARY:

- ❖ Proficient in C, C++ programming, and Python Scripting.
- ❖ Familiar with communication protocols: UART, SPI, I²C, GPIO, CAN, LIN.
- ❖ Proficient in designing, synthesizing and debugging embedded systems on FPGAs in bare metal as well as multi-threaded real-time environment.
- ❖ Hands-on experience in building projects on development boards like Xilinx Nexys 4DDR FPGA, Arduino, Raspberry Pi, Beaglebone Blackboard, GSM/GPRS SIM 900A modem, GPS-NEO-6M, SD Card Module, Wi-Fi module ESP8266, RedBearLab BLE Nano and ARM7 LPC2148, LPC1768.
- ❖ Prior experience in developing Linux device drivers and APIs for various embedded applications.
- ❖ Experience in HDLs and HVLs like Verilog and SystemVerilog respectively.
- ❖ Strong interpersonal skills and ability to work efficiently in a team environment.

EDUCATION

- **M.S in Electrical and Computer Engineering,** Portland State University, Oregon — September'16 – June'18
  Major Courses: Microprocessor System Design, Advanced Computer Architecture – I, II, Embedded System Design with FPGAs, Fundamentals of Operating System, Embedded System Programming, Data Structures and Algorithms, System-on-chip (SoC) Design with FPGA's.
- **B.E in Electronics and Telecommunication Engineering,** Dr. B. A. Marathwada University, India — August'11– July'15

WORK EXPERIENCE

Xilinx – Embedded Software Engineer – San Jose, CA, USA — October'18 – Present

- Developing Bare Metal and Linux drivers for AI-Engine components using Xilinx ACAPs. Implementing APIs for interrupt-handling for AI- Engine.
- Contributing to the architecture and design of the overall embedded software stack for AI-Engine solutions.
- Developing heterogeneous memory management solutions for asynchronous multi-processing platforms. Optimizing the solutions developed for performance and designing them for scalability.
- Contributing to all the phases of software development, from requirement gathering, analysis, design, development, testing and final release to customers.
- Working with different teams to identify problems and delivering software solutions in line with product roadmap on time with high quality.

HDL Express – Design and Verification Volunteer – Canby, OR, USA — August'18 – September '18

- Designing, testing, and debugging of a new Out of Order CPU based on a new method of dynamic instruction scheduling called the TIP Algorithm.
- Simulation, documentation, and possibly research into tools that may be used to aid in this development effort.

Tesla Inc. - Firmware Engineering Intern – Palo Alto, CA, USA — November'17 – June'18

- Developing firmware for ARM-based CAN router to inject faults, modify/corrupt CAN message or make ECUs go MIA.
- Adding capabilities to enable existing dyno platform to validate the Electronic Stability Programme (ESP) and Brake Booster (iBooster) functionality at the system level.
- Creating a testing framework to automate firmware validation of Redundant Electronic Brake Request (R-EBR) feature on Dyno platform.
- Designing and implementing a state machine models for the vehicle lock system for automated firmware validation. Developing hardware to integrate the behavioral models in the existing testing framework such that it guarantees precise control over various security components.
- Developing a Jenkins pipeline to detect new firmware builds, OTA update them on a vehicle, test critical features and upload results for nightly automation testing.

Sharpe Energy Solutions - Embedded Systems Intern – Portland, OR, USA — September'17 – November'17

- Developing an open source control platform to track the location of the sun based on different sensor data extracted locally.
- Translating given requirements to an actual working prototype. Interfacing Wi-Fi chip to send/receive critical alert messages during extreme weather conditions. During normal operation, the current state of solar panel and sensor data was logged on a remote server.
- Improving the existing system with more reliable and scalable solutions for a market ready product.

TECHNICAL QUALIFICATIONS

- **Languages** : C, C++, Python, x86 Assembly, SystemVerilog, Verilog.
- **Tools** : Xilinx Vivado and SDK, ARM Keil MDK, Arduino, Linux device drivers, FreeRTOS, Jenkins, Questasim, LabView, MATLAB.

ACADEMIC PROJECTS

Hand gesture controlled wireless robot – C, Verilog, Xilinx Nexys, FPGArduino, ESP 8266 WiFi module, OpenCV, Python — March'17

- Designed an algorithm in Python using OpenCV libraries to detect the number of fingers present in real-time within a predefined contour.
- Devised a fast control system on Xilinx Nexys 4 DDR board, which generates control signals based on the hand gestures captured in real-time.
- Established UART communication between laptop and Nexys board to deliver proper information based on the hand gesture.
- Ported MIPS based Arduino core to Xilinx Nexys4DDR FPGA board and made use of Bridge libraries to virtually map the pins of the robot.

RTOS driven closed loop control system – C, Verilog, Xilinx Nexys, XilKernel, Xilinx Vivado, SDK, ARMmbed SerialPortPlotter — February'17

- Implemented a full **PID controller** for an electric motor with and without load. Created a custom IP for interfacing PmodHBridge with Nexys FPGA. Wrote device drivers for peripheral used which includes PmodHbridge, PmodOLED display, and PmodENC rotary encoder.
- Synthesized hardware for PWM generation and edge detection, for driving the motor and to obtain the actual speed from the pulses generated by Hall effect sensor respectively. AXI bus interface was used to communicate data between the HW blocks and Microblaze CPU.
- Created a multithreaded PID control application that runs on a lightweight real-time operating system "Xilkernel" using IPC mechanisms like semaphore and message queue.

PAg and gshare Branch Predictor – C++ — November'17

- Implemented PAg and gshare branch predictor for an existing simulator in C++. Analyzed the % IPC improvement over baseline bimodal predictor for different benchmark.